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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,887	11/16/2001	Ryuta Tanaka	1075.1181	7579

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EXAMINER	
SHAH, NILESH R	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/987,887	TANAKA ET AL.	
	Examiner	Art Unit	
	Nilesh Shah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-46 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neches (4,445,171) in view of Raz et al (5,860,137) (hereinafter Raz)

4. As per claim 1, Neches teaches the invention substantially as claimed including a multiprocessor system comprising:

   two or more processor elements whose performances are to be executed by a common program (col. 6 lines 1-34;col. 51 lines 6-22).

5. Neches does not specifically teach the use of a switching between processors. Raz teaches a control section for switching said one processor element to said another processor element for execution by said common program (abstract; col.1 lines 55-67; col.11 lines 5-29);

a switching request signal detecting section for detecting a switching request signal to request switching such plural processor elements one from another (col. 8 lines 12-45; col. 7 lines 24-40; col. 9 lines 10-40);

a storing section. responsive to each switching of said processor elements by said control section, for storing handover information relating to the common program which information is to be handed over from said one processor element to said another processor element (col. 13 lines 1-6;col.11 lines 5-29);

a store control section for storing said handover information from said one processor element into said storing section when said switching request signal detecting section detects the switching request signal (col. 1 line 55- col. 2 line 21; col. 10 line 59- col.11 line 30);

a stop control section for stopping the performance of said one processor element after said store control section stores said handover information into said storing section (col. 13 lines 26-35;col. 13 lines 1-6;col.11 lines 5-29).;

a start control section for starting the performance of said another processor element using said handover information stores in said storing section (col. 2 lines 40-60; ; col. 10 line 59- col.11 line 30).

6. It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Neches and Raz because Raz's method of switching between processors would improve Neches system by allowing more than one process to work on a task thereby improving the overall system.

7. As per claim 3, Raz teaches a multiprocessor wherein if a performance requested to be executed for one of said plural processor elements is to be made by another processor element, said last-named one processor element outputs said switching request signal to said control section. (col. 9 lines 41-51).

8. Claim 4 is rejected based on the same rejection as claim 3 above.

9. As per claim 5, Raz teaches a multiprocessor wherein said switching request signal is a switching control interruption signal (col. 11 lines 1-15).

10. Claim 6 is rejected based on the same rejection as claim 5 above.

11. As per claim 7, Raz teaches a multiprocessor wherein upon receipt of a signal from outside said system, said control section outputs an interruption signal to the last-named another processor element to stop the performance thereof (col. 9 lines 41-51; col. 13 lines 26-35;col. 13 lines 1-6;col.11 lines 5-29).

12. Claims 8-12 are rejected based on the same rejection as claim 7 above.

13. As per claim 13, Raz teaches a multiprocessor

wherein said control section has a table for indicating, for designation of one at a time from said plural processor elements, a permitted-to-perform processor

element, which is allowed to perform processing, and controls the switching of said processor elements so

as to designate said permitted-to-perform processor element based on said table (col. 10 lines 45-57; col. 13 lines 26-35; col. 5 lines 13-25; col. 3 lines 45-47;col. 6 lines 33-37).

14. Claims 14-24 are rejected based on the same rejected as claim 13 above.

15. As per claim 25, Raz teaches a multiprocessor with consulting said table, said control section selects said permitted-to-perform processor element, which is indicated by said table, as said another processor element, and outputs an interruption signal to said permitted-to-perform processor element to stop the performance thereof (col. 5 lines 13-25; col. 3 lines 45-47;col. 6 lines 33-37).

16. Claims 26-36 are rejected based on the same rejection as claim 25 above.

17. As per claim 37, Raz teaches a multiprocessor wherein said control section actuates one of said plural processor elements with precedence over the remaining processor elements and actuates one of said remaining processor elements in place of the second-to-last-named one processor element as demand arises (col. 2 lines 7-21; col. 5 lines 13-25; col. 3 lines 45-47;col. 6 lines 33-37).

18. As per claim 38, Neches teaches a multiprocessor wherein said plural processor elements are different in function from one another (col. 5 lines 1-40).

19. As per claim 39, Raz teaches a multiprocessor wherein, upon receipt of a signal from outside said system, said control section selects from said plural processor elements one processor element to handle the last-named signal and actuates the selected one processor element (col. 5 lines 13-25; col. 3 lines 45-47;col. 6 lines 33-37).

20. As per claim 40, Raz teaches a multiprocessor system wherein at least one of said plural processor element is an MPU (Micro Processing Unit) and the remainder is a DSP (Digital Signal Processor), or vice versa (col. 3 lines 21-65).

21. Claim 41 is rejected based on the same rejection as claim 40 above.

22. As per claim 42, Raz teaches a multiprocessor system further comprising an invalidating section for invalidating the switching function of said control section to thereby actuate at least two or more of said plural processor elements simultaneously (col. 3 lines 24-35)

23. As per claim 43, Raz teaches a multiprocessor system wherein said handover information to be stored in said storing section includes at leas t one selected from

the group consisting of a value of a program counter an argument of a function a return value of a function and content of a stack pointer (col. 5 lines 37-63).

24. As per claim 44, Neches teaches a multiprocessor control method for switching two or more processor elements of a multiprocessor system, whose performances are to be executed by a common program, said control method comprising the steps of (col. 6 lines 1-34;col. 51 lines 6-22).

Raz teaches detecting a switching request signal to request switching such plural processor element, one from another (col. 10 line 59- col.11 line 30; col. 13 lines 26-35;col. 13 lines 1-6;col.11 lines 5-29);

in response to each switching of said processor elements, storing handover information relating to the common program, which information is to be handed over from said one processor element to said another processor element, into a storing section of said multiprocessor system(col. 5 lines 13-25; col. 3 lines 45-47;col. 6 lines 33-37); and after said handover information has been stored into the storing section, stopping the performance of said one processor element and starting said another processor element using said handover information stored in the storing section (col. 10 lines 45-57; col. 13 lines 26-35; col. 5 lines 13-25; col. 3 lines 45-47;col. 6 lines 33-37).

25. Claim 45 is rejected based on the same rejection as claim 44 above.

26. Claim 46 is rejected based on the same rejection as claim 1 and 44 above.

Response to Arguments

27. Applicant's arguments filed 9/19/05 have been fully considered but they are not persuasive.

28. Applicant argues that Raz does not teach a switching method.

29. Examiner respectfully disagrees with applicant's remarks. Raz teaches a switching method (col. 2 lines 40-60; ; col. 10 line 59- col.11 line 30) 'To fully implement the above-described load balancing technique in this system, a programmable switching mechanism is added to the data storage system. The programmable switching mechanism enables the managing host processor through commands which it send to the data storage system to reconfigure the data storage system by changing the set of logical volumes that are connected to each host connection.'

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will

be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2195

NS
November 18, 2005

MENGAL T. AN
SUPERVISORY PATENT EXAMINER
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